A

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. **0100.990020**
Total Pages 31
First Inventor or Application Identifier Oleg Drapkin et al.
Title SINGLE GATE OXIDE DIFFERENTIAL RECEIVER AND METHOD
Express Mail Label No. EJ354676058US

APPLICATION ELEMENTS *See MPEP chapter 600 concerning utility patent application contents.*	*ADDRESS TO:* **Assistant Commissioner for Patents Box Patent Application Washington, DC 20231**

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. ☒ Specification *Total Pages* 15
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawings *(35 USC 113) Total Sheets* 4
4. Oath or Declaration *Total Pages* 2
a. ☒ Newly executed (original or copy)
b. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program *(Appendix)*
6. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (cover sheet & document(s))
8. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☐ Power of Attorney
9. ☐ English Translation Document (if applicable)
10. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☐ Small Entity Statement(s) ☐ Statement filed in Prior Application, Status still proper and desired.
14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. ☐ Other

16. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No:
Prior Application Information: Examiner *Group / Art Unit:*

17. CORRESPONDENCE ADDRESS

☐ *Customer Number or Bar Code Label* or, ☒ *Correspondence Address Below*

Markison & Reckamp, P.C.
175 West Jackson Boulevard - Suite 1015
Chicago, Illinois 60604
Telephone:312-939-9800 **Facsimile: 312-939-9828**

Name (Print/Type)	**Christopher J. Reckamp**	REGISTRATION NUMBER	**34,414**
Signature		Date	**December 14, 1998**

FEE TRANSMITTAL

Note: Effective October 1, 1997.
Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 800

Complete if Known

Application Number	
Filing Date	**December 14, 1998**
First Named Inventor	**Oleg Drapkin et al.**
Group Art Unit	
Examiner Name	
Attorney Docket Number	**0100.990020**

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number	50-0441
Deposit Account Name	**ATI Technologies, Inc.**

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Charge the Issue Fee Set in 37 CFR 1.18 at the mailing of the Notice of Allowance

2. ☐ Payment Enclosed:
☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	760	201	380	Utility filing fee	**760**
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	760	208	380	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 760

2. CLAIMS

Claims	Extra	Fee from below	Fee Paid
Total 17	(-20 =) 0	18	**0**
Indep. 3	(- 3 =) 0	78	**0**
Multiple Dep.			

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim
109	78	209	39	Reissue independent claims over original patent
110	18	210	9	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension for reply within second month	
117	870	217	435	Extension for reply within third month	
118	1,360	218	680	Extension for reply within fourth month	
128	1,850	228	925	Extension for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	**40**
146	760	246	380	Filing a submission after final rejection (37 CFR 1.129(a))	
149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify)					
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	**Christopher J. Reckamp**			Reg. Number	**34,414**
Signature		Date	**December 14, 1998**	Deposit Account User ID	

PATENT APPLICATION

Attorney Docket No. 0100.990020

SINGLE GATE OXIDE DIFFERENTIAL RECEIVER AND METHOD

Related Co-pending Applications

This is a related application to the following co-pending applications, filed on even date, having the same inventors and assigned to instant assignee:

1. Differential Input Receiver and Method for Reducing Noise, having serial number _____ and attorney docket no. 0100.990019;
2. Voltage Supply Discriminator and Method, having serial number _____ and attorney docket no. 0100.990017; and
3. Pre-buffer Voltage Level Shifting Circuit and Method, having serial number _____ and attorney docket no. 0100.990018.

Field Of The Invention

The invention relates generally to integrated circuit signal receivers and more particularly to differential receivers.

Background Of The Invention

Graphics controller chips, like many integrated circuit devices, utilize CMOS, logic cores, and associated input/output (I/O) pads as part of their circuit makeup. I/O pads include, for example, input/output buffers coupled to a common pad or pin. There is a constant challenge to continuously design smaller, faster and more complicated integrated circuits to provide increased functionality for multimedia applications and other applications. Typically, the logic core operates at a different supply voltage than the I/O pads. For example, with logic cores having gate lengths of .25 um, a core logic

supply voltage may be 2.5 volts. Corresponding supply voltages for the input/output pads, however, may be different supply voltages such as 3.3 volts. However, future generation chips require faster speeds and lower power consumption, hence, lower supply voltages so that the I/O pads can switch at faster frequencies.

Also, integrated circuits must often provide compatibility with older versions of interface circuits. As a result, an integrated circuit may require that the I/O pads operate at either a 3.3 volt level, or for example, at a lower 1.5 volt level. The gate length and gate oxide thickness of I/O pad transistors must also typically be decreased to provide faster circuits that draw less current. With multilevel supply voltages, multi-gate oxide devices are often used to provide the requisite logic levels and overvoltage protection. However, a problem arises when multi-gate oxide transistors are used on the same chip. Using differing gate oxide thickness' requires additional fabrication processes and, hence, results in higher fabrication costs. Moreover, the larger gate oxide thickness' can slow the device down unnecessarily. For low voltage CMOS signaling, the input/output pad must also be designed to prevent static leakage and prevent damage due to gate-source or gate-drain overvoltage.

FIG. 1 shows a block diagram of a conventional I/O pad 10 including an output buffer 12 and an input buffer 14 coupled to a common pad or pin 16. The I/O pad 10 communicates signals to and from the pad 16 for the core logic 18. Some integrated circuit interfaces such as interfaces that interface a graphics controller chip with other processing chips (e.g. AGPX and AGP2X) for example are required to work with a 3.3 volt I/O voltage supply as well as with a 1.5 voltage supply. At the same time, the core voltage supply for .25 micron technology is 2.5 volts. This typically means that the input signal received by the interface chip can have a 0 volt to 1.5 volt swing for one application and 0 volt to 3.3 volt swing for another application. Where thick gate oxide MOS transistors are used for 3.3 volt I/O voltage supplies, they are typically unsuitable for 1.5 voltage supply based circuits because they cannot provide the required timing parameters since they may be too slow at the 1.5 voltage supply. In addition, thin gate oxide MOS transistors cannot typically withstand the 3.3 volt supply for a 3.3 volt input

signal environment since a gate-source or gate-drain junction may have a 3.3V potential during normal operation. This may be higher than the normal maximum operating voltage for the device. It has been recommended to use a differential input stage to meet timing parameters and to make these parameters less dependent on temperature and less susceptible to noise.

A common solution to accommodate multiple differing supply voltages for a receiver stage for an I/O pad or other circuit for example has been to make two different integrated circuit chips - one for the 3.3 volt supply and another chip for a 1.5 volt supply. Typically, single (or thin gate) gate oxide differential receivers are designed for 1.5 volt supplies and for 1.5 volt input signals and are on a separate integrated circuit from thick gate oxide differential receivers. Thick gate oxide differential receivers are used to accommodate the 3.3 volt voltage supply for a 3.3 input signal. As such, there are typically two different designs on two different integrated circuit chips.

Consequently, there exists a need for a differential receiver and circuitry that accommodates a varying voltage supply that automatically accommodates different supply voltages and input signal levels on a single integrated circuit chip. Moreover, it would be desirable if such a differential receiver was able to automatically switch supply voltages and be designed as a single gate oxide circuit.

Brief Description Of The Drawings

FIG. 1 is a block diagram illustrating a prior art integrated circuit with core logic and an I/O pad having an input buffer (receiver), and an output buffer.

FIG. 2 is a block diagram illustrating one embodiment of an integrated differential receiver in accordance with one embodiment of the invention.

FIG. 3 is a circuit diagram illustrating one embodiment of an integrated differential receiver in accordance with the invention wherein a differential receiver and associated switchable voltage supply circuit are made from single gate oxide devices.

FIG. 4 is another embodiment of an integrated differential receiver in accordance with the invention wherein the differential receiver is a single gate oxide device and a switchable voltage supply circuit is a thick gate oxide based circuit.

Detailed Description Of a Preferred Embodiment of The Invention

Briefly, an integrated differential receiver includes a single gate oxide differential receiver and an associated switchable voltage supply circuit. The integrated differential receiver determines the desired receiver supply voltage and selects a supply voltage for the single gate oxide differential receiver. When a lower supply voltage is determined as the desired supply voltage, the integrated differential receiver automatically provides a supply voltage to the single gate oxide differential receiver with a voltage higher than the I/O pad supply voltage and higher than the maximum input signal voltage to increase the speed of operation for the differential receiver. The switchable voltage supply circuit is operatively responsive to a control signal which indicates the desired supply voltage for the I/O pad. In one embodiment, both the single gate oxide differential receiver and the switchable voltage supply circuit are single gate oxide circuits.

In an alternative embodiment, the switchable voltage supply circuit is a thick gate oxide based circuit and is used to selectively supply a supply voltage to the single gate oxide differential receiver. In both embodiments, a supply voltage to the differential receiver is selected to be different from an I/O pad supply voltage when the desired I/O pad supply voltage is below a predetermined threshold or reference voltage.

FIG. 2 illustrates one embodiment of an integrated differential receiver 100 having a single gate oxide differential receiver 102, a switchable voltage supply circuit 104 and an isolation output buffer 106. The switchable voltage supply circuit 104

receives as input, a desired I/O pad supply voltage 108 which may be a plurality of different supply voltages. For purposes of illustration only, the desired supply voltages may be, for example, 3.3 volts and 1.5 volts. The switchable voltage supply circuit 104 also receives another input such as a first reference voltage 110 which may be for example the supply voltage for the core logic, such as 2.5 volts or other suitable reference voltage. In addition, the switchable voltage supply circuit 104 receives a control signal 112 which indicates an input signal voltage range, such as whether the input signal 114 to the differential receiver 102 will be in a range from 0 to 1.5 volts, or for example 0 to 3.3 volts. The control signal may be a signal from an input pin for the integrated circuit or may come from other suitable control logic on the integrated circuit. The switchable voltage supply circuit 104 selects a single gate oxide differential receiver supply voltage 116 for the single gate oxide differential receiver 102 based on the desired I/O pad supply voltage 108, the first reference voltage 110 and the control signal 112.

The differential receiver 102 receives the input signal 114, for example, from an external chip. The input signal is received on one input of the single gate oxide differential receiver 102. On another input, the single gate oxide differential receiver 102 receives a second reference voltage 117. The second reference voltage 117 may be for example one half of the desired supply voltage 108, or any other suitable reference voltage. Based on the second reference voltage 117 and the level of the input signal 114, the differential receiver outputs a received signal 118 to the isolation output buffer 106. The isolation output buffer 106 then outputs the signal 118 to the core logic.

In operation, the circuit provides either of at least an I/O pad supply voltage and a second reference supply voltage for the single gate oxide differential receiver based on the control signal such that the reference supply voltage is selected as the differential receiver supply voltage when the control signal indicates a maximum input signal voltage to be less than the second reference voltage. The circuit also provides the I/O pad supply voltage as the differential receiver supply voltage when the control signal indicates a maximum input signal voltage to be greater than the second reference voltage.

Accordingly, the switchable voltage supply circuit determines a desired I/O pad supply voltage and the input voltage range and generates a single gate oxide receiver supply voltage to maximize the speed of operation of the differential receiver 102. For example, if the desired supply voltage 108 is set at 3.3 volts, and the control signal 112 indicates that the input signal range is 0 to 3.3 volts, the switchable voltage supply circuit 104 will generate a 3.3 volt supply for the single gate oxide differential receiver 102. It will be recognized that the supply voltage to the single gate oxide differential receiver 102 may not be exactly 3.3 volts, or the indicated input signal level, but it may be different by an order of several junction thresholds depending upon the design of a switchable voltage supply circuit 104.

If however the desired I/O pad supply voltage is 1.5 volts as indicated by the I/O pad voltage 108, and as the control signal 112 indicates that the input voltage range is 0 to 1.5 volts, the switchable voltage supply circuit 104 selects a supply voltage 116 for the single gate oxide differential receiver that is different from the 1.5 volt I/O pad supply or input signal range. For example if the I/O pad 108 is indicated to be 1.5 volts by the control signal, the switchable voltage supply circuit 104 generates a 2.5 volt single gate oxide differential receiver supply voltage 116 for the differential receiver to maximize the speed of operation of the differential receiver 102. As such when a lower I/O pad supply voltage is used, the integrated differential receiver 100 automatically detects the level and outputs a higher supply voltage to the single gate oxide differential receiver. In one embodiment, the higher output voltage is equal to the first reference voltage.

FIG. 3 shows a circuit diagram of one embodiment of the integrated differential receiver 100 wherein the switchable voltage supply circuit 104 is also based on single gate oxide devices such as nmos and pmos field effect transistors (FETS), or any other suitable devices. The switchable voltage supply circuit 104 includes a pair of current sources 200a and 200b wherein one current source is used to supply one level of supply voltage to the single gate oxide differential receiver 102 and the other current source is used to provide the requisite current (and hence voltage) for a second supply voltage for the single gate oxide differential receiver. The switchable voltage supply circuit 104

includes a first voltage switching circuit 202 and a second switching circuit 204. The first switching circuit 202 is switched in and provides a higher source voltage such as 3.3 volts, whereas the second switching circuit 204 switches in a supply voltage higher than the maximum input voltage. For example, when the maximum input voltage is 1.5 volts, the switching circuit 204 switches in a higher reference voltage, than the maximum input voltage, such as 2.5 volts, to supply the voltage for the single gate oxide differential receiver. As shown, all FET devices are thin gate oxide devices. In addition all of the FET devices for the single gate oxide differential receiver are also thin gate devices, such as silicon dioxide based FETs having a gate oxide thickness of approximately 50 angstroms.

The voltage switching circuit 202 includes a plurality of pmos transistors 206, 208 and 210, and a nmos transistors 212, and 214. Similarly, the second voltage supply circuit 204 includes pmos transistors 216, 218 and 220, and nmos transistors 222 and 224. A pair of inverters 226 and 228 are also used. The switchable voltage supply circuit 104 is a single gate oxide device in part because of nmos transistors 214 and 224. These devices serve as a type of voltage divider. The nmos transistor 214 is "on" and nmos transistor 224 is "off" when there is a 3.3V input signal since the control signal 112 is 0V. For a 1.5V condition, the control signal 112 is equal to 2.5V. Therefore, nmos transistor 214 is "off" and nmos transistor 224 is "on." When nmos transistor 214 is "on" and nmos transistor 224 is "off", switching circuit 202 is "on", sending current to node1 from the 3.3V voltage supply, and switching circuit 204 is "off".

When nmos transistor 214 is "off", and nmos transistor 224 is "on", switching circuit 204 is "on" sending current to node1 from the 2.5V supply, and switching circuit 202 is "off". In this case, the gate of nmos transistor 214 has a potential of 0 volts, but the drain of pmos transistor 206 might have a potential of 3.3V. Therefore, nmos transistor 212 prevents nmos transistor 214 from having its gate-drain voltage of 3.3V. The gate potential of nmos transistor 212 is 2.5V. This results in the potential of its source will not be larger than 2.5V-Vtn (when the switching circuit 202 is off). The nmos transistor 222 serves the same purpose when the switching circuit 204 is "off".

In operation, the inverter 226 receives the control signal 112 which, by way of example, may vary from 0 volts to 2.5 volts. In this example, the control signal is 0 volts, when a 3.3 volt I/O pad supply is used. The control signal is 2.5 volts when the I/O pad supply voltage is 1.5 volts. When the I/O pad supply voltage is 3.3 volts, the control signal, being 0 volts, becomes inverted through inverter 226 to a 2.5 volt level turning on nmos transistor 214. This in turn turns on transistor 212 which then activates the current source 200a to supply approximately 2.8 volts as a supply voltage for the single gate oxide differential receiver at node 1. The control signal having been once inverted through inverter 226 is again inverted through inverter 228. As such, the output of inverter 228 is in a logic low level thereby keeping transistors 224 off which in turn through transistor 222, keeps the current source 200b off. The transistors 212 and 222 provide a type of voltage divider to allow single gate oxide technology to be used for all transistor devices in the circuit since the gate to source and gate to drain voltages do not exceed maximum allowable voltage levels and thereby are not degraded due to overvoltage conditions when a I/O pad supply voltage is for example 3.3 volts.

Conversely, when the control signal 112 is in a logic high level, such as 2.5 volts, indicating that the I/O pad supply voltage is 1.5 volts or other level lower than a previous level, the inverted signal through inverter 226 shuts off transistor 214 and turns on transistor 224. This in turn shuts off the current source 200a and activates the current source 200b. With the current source 200b activated, a voltage level at node 1 of approximately 2.0 volts is supplied as the single gate oxide differential receiver supply voltage. The voltage switching circuits 202 and 204 operate to alternately activate the common current source to selectively provide the differential receiver supply voltage for the single gate oxide differential receiver. Transistors 206,208 and 210 provide the potential of well2 equal to 3.3V when the switching circuit 202 is "on" as well as provide floating conditions for well1, and switch "off" transistors 216, 218 and 220. Transistors 216, 218 and 220 provide well1 with a potential equal to 2.5Vwhen the switching circuit 204 is "on" as well as provide floating conditions for well2 and switching "off" transistors 206, 208 and 210.

The single gate oxide differential receiver 102 includes differential input pmos transistors 230 and 232 as well as nmos transistors 234 and 236. In addition, pmos transistor 238 has a gate coupled to the first reference voltage and a source coupled to the single gate oxide differential receiver supply voltage 116. A drain is coupled to the drain of pmos input transistor 232 that receives the input signal. In operation, the transistors 230 - 236 operate as a conventional differential receiver. However, the transistor 238 acts to effectively provide the drain voltage of transistor 236 at the level of Vtn when input transistor 232 is off. For example, if the input voltage range was 0 to 3.3 volts for I/O pad supply voltage of 3.3 volts, when the input signal is 3.3 volts, transistor 232 is turned off and transistor 238 pulls up the drain of transistor 236 to reduce noise and also prevents the gate to drain voltage of transistor 232 from experiencing a voltage condition that exceeds a normal operating voltage range since the drain does not reach 0 volt level during a 3.3 volt or higher input voltage range. As such, the disclosed circuit provides a single gate oxide solution to reduce fabrication costs while still providing a robust design over differing I/O pad supply voltage ranges and input signal input signal voltage ranges.

FIG.4 shows another embodiment of an integrated differential receiver 300 wherein the switchable voltage supply circuit 302 uses thick gate oxide transistors. Another difference is that a plurality of control signals 304 and 306 are used as opposed to a single control signal. The single gate differential receiver circuit 102 is identical to that previously described with reference to FIG. 3. The switchable voltage supply circuit 302 includes a current source 308 as well as two pairs of thick gate oxide pmos FET 310, 312, 314 and 316. The thick gate oxide devices may have for example a gate oxide thickness of approximately 70 angstroms. The pair of pmos FETs 310 and 312 act to supply the current source with a high supply voltage, such as 3.3 volts, when the I/O pad supply voltage is 3.3 volts. The pair of pmos transistors 314 and 316 serves to provide a current source when the I/O pad supply voltage is 1.5 volts (a lower supply voltage). In operation, when the control signal is at a logic low level, for example when the I/O pad supply voltage is the higher supply voltage such as 3.3 volts, the pmos transistors 310 and 312 are turned on. To provide 3.3V at node1, nmos transistor 308 works like a current

source for the differential receiver. Its gate is biased with VREF2 (half of 3.3V or half of 1.5V).

When the input to transistors 310 and 312 is low, these transistors are on and the gates of transistors 314 and 316 are high through inverter 320. As such, they are effectively turned off and isolated. When the control signal is a logic high, such as 2.5 volts when the I/O pad supply voltage is a lower voltage such as 1.5 volts, the pair of transistors 310 and 312 are effectively shut off but the transistors 314 and 316 are turned on thereby pulling node 1 to approximately 2.5 volts.

It should be understood that the implementation of other variations and modifications of the invention in its various aspects will be apparent to those of ordinary skill in the art, and that the invention is not limited by the specific embodiments described. It is therefore contemplated to cover by the present invention, any and all modifications, variations, or equivalents that fall within the spirit and scope of the basic underlying principles disclosed and claimed herein.

Claims

WHAT IS CLAIMED IS:

1. An integrated differential receiver for an input/output pad comprising:

a single gate oxide differential receiver; and

a switchable voltage supply circuit, operatively coupled to the single gate oxide differential receiver, switchable through at least one control signal to select a differential receiver supply voltage for the single gate oxide differential receiver wherein at least one of the selected supply voltages is different from an input/output pad supply voltage.

2. The receiver of claim 1 wherein the switchable voltage supply circuit selects the differential receiver supply voltage that is a higher voltage than the I/O pad supply voltage.

3. The receiver of claim 1 including an isolation output buffer operatively coupled to a receiving circuit that outputs a signal.

4. The receiver of claim 1 wherein the differential receiver receives a first reference voltage on a first differential input and an input voltage on a second differential input and wherein the switchable voltage supply circuit selects the differential receiver supply voltage for the single gate oxide differential receiver to be a voltage level higher than a maximum voltage level of the input voltage.

5. The receiver of claim 1 wherein the switchable voltage supply circuit provides either of at least an I/O pad supply voltage and a second reference supply voltage for the differential receiver based on the control signal such that the reference voltage is selected as the differential receiver supply voltage when the control signal indicates a maximum input signal voltage to be less than the second reference voltage, and wherein the switchable voltage supply circuit provides the I/O pad supply voltage as the differential

receiver supply voltage when the control signal indicates a maximum input signal voltage to be greater than the second reference voltage.

6. The receiver of claim 1 wherein the switchable voltage supply circuit is operatively responsive to at least two control signals.

7. The receiver of claim 1 wherein the single gate oxide differential receiver includes a transistor, operatively coupled to an input transistor of a single gate differential input stage having a gate coupled to the first reference voltage, a source coupled to the single gate oxide differential receiver supply voltage, a drain coupled to a drain of the input transistor that receives the input signal.

8. The receiver of claim 1 wherein the receiver generates an output signal to circuitry for a video graphics processor.

9. The receiver of claim 1 wherein the switchable voltage supply circuit includes a plurality of voltage switching circuits operative to alternately activate a common current source to selectively provide the differential receiver supply voltage for the single gate oxide differential receiver.

10. An integrated differential receiver for an input/output pad comprising:

a single gate oxide differential receiver that receives a first reference voltage on a first differential input and an input voltage on a second differential input;

a switchable voltage supply circuit, operatively coupled to the single gate oxide differential receiver, switchable through at least one control signal to select a differential receiver supply voltage for the single gate oxide differential receiver wherein at least one of the selected supply voltages is a voltage level higher than a maximum voltage level of the input voltage; and

an isolation output buffer operatively coupled to core logic.

11. The receiver of claim 10 wherein the switchable voltage supply circuit provides either of at least an I/O pad supply voltage and a second reference supply voltage for the differential receiver based on the control signal such that the reference voltage is selected as the differential receiver supply voltage when the control signal indicates a maximum input signal voltage to be less than the second reference voltage, and wherein the switchable voltage supply circuit provides the I/O pad supply voltage as the differential receiver supply voltage when the control signal indicates a maximum input signal voltage to be greater than the second reference voltage.

12. The receiver of claim 11 wherein the switchable voltage supply circuit is operatively responsive to at least two control signals.

13. The receiver of claim 11 wherein the single gate oxide differential receiver includes the single gate oxide differential receiver includes a transistor, operatively coupled to an input transistor of a single gate differential input stage having a gate coupled to the first reference voltage, a source coupled to the single gate oxide differential receiver supply voltage, a drain coupled to a drain of the input transistor that receives the input signal.

14. A method for controlling a voltage supply for a differential receiver comprising the steps of:

providing either of at least an I/O pad supply voltage and a second reference supply voltage for a single gate oxide differential receiver based on a control signal such that the reference supply voltage is selected as the differential receiver supply voltage when the control signal indicates a maximum input signal voltage to be less than the second reference voltage, and

providing the I/O pad supply voltage as the differential receiver supply voltage when the control signal indicates a maximum input signal voltage to be greater than the second reference voltage.

15. The method of claim 14 including the step of buffering an output signal from the single gate oxide differential receiver prior to the output signal being received by core circuitry.

16. The method of claim 14 including receiving a first reference voltage on a first differential input and an input voltage on a second differential input and selecting the differential receiver supply voltage for a single gate oxide differential receiver to be a voltage level higher than a maximum voltage level of the input voltage.

17. The method of claim 14 including providing either of at least an I/O pad supply voltage and a second reference supply voltage for a differential receiver based on the control signal such that the reference voltage is selected as the differential receiver supply voltage when the control signal indicates a maximum input signal voltage to be less than the second reference voltage, and providing the I/O pad supply voltage as the differential receiver supply voltage when the control signal indicates a maximum input signal voltage to be greater than the second reference voltage.

SINGLE GATE OXIDE DIFFERENTIAL RECEIVER AND METHOD

Abstract Of The Invention

An integrated differential receiver includes a single gate oxide differential receiver and an associated switchable voltage supply circuit. The integrated differential receiver determines the desired receiver supply voltage and selects a supply voltage for the single gate oxide differential receiver. When a lower supply voltage is determined as the desired supply voltage, the integrated differential receiver automatically provides a supply voltage to the single gate oxide differential receiver with a voltage higher than the I/O pad supply voltage and higher than the maximum input signal voltage to increase the speed of operation for the differential receiver. The switchable voltage supply circuit is operatively responsive to a control signal which indicates the desired supply voltage for the I/O pad. In one embodiment, both the single gate oxide differential receiver and the switchable voltage supply circuit are single gate oxide circuits.

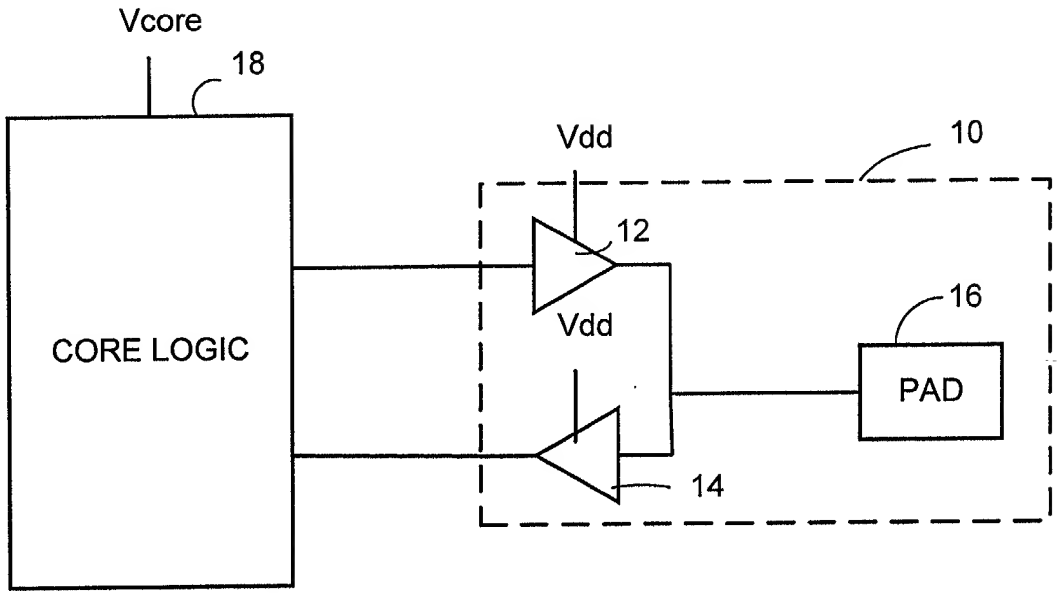

FIG. 1
(PRIOR ART)

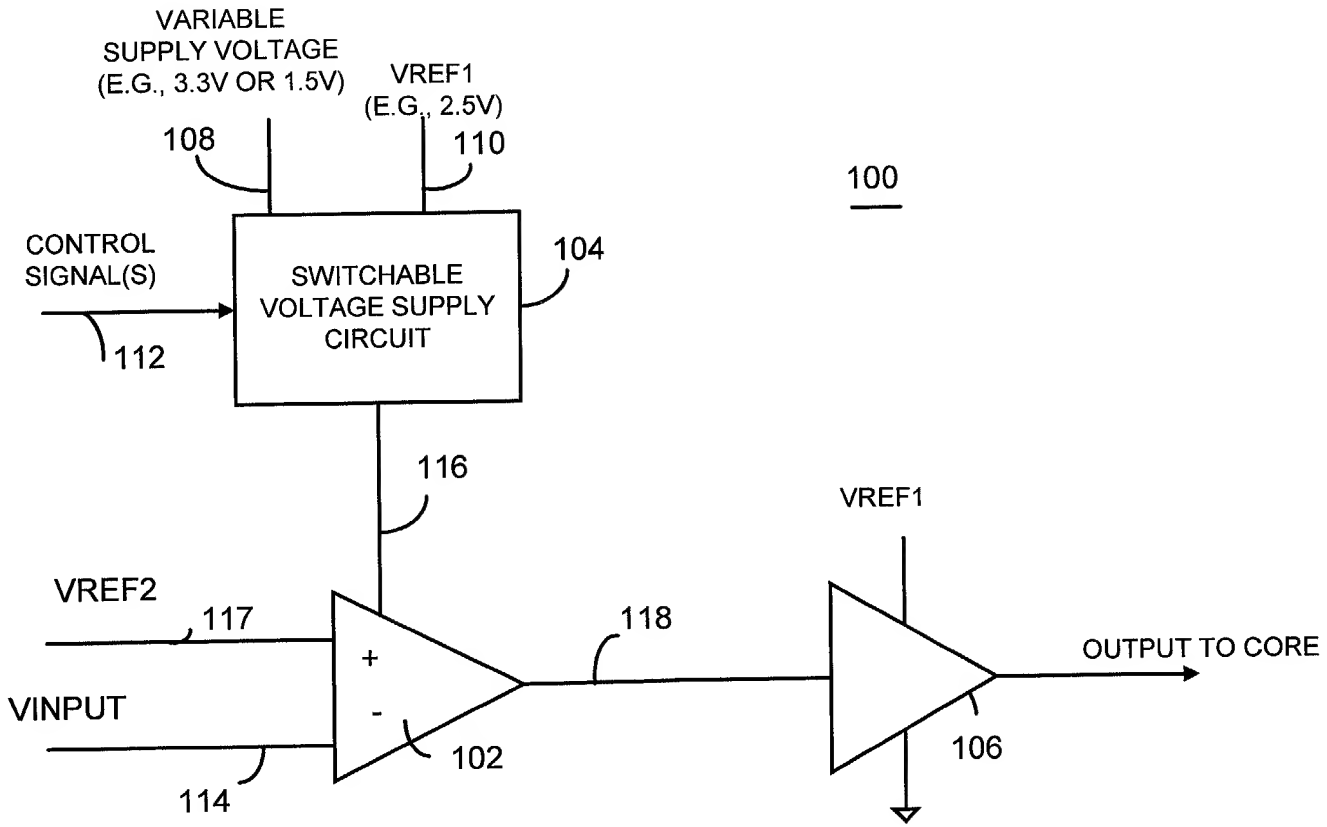
VARIABLE
SUPPLY VOLTAGE
(E.G., 3.3V OR 1.5V)
108
VREF1
(E.G., 2.5V)
110
100
CONTROL
SIGNAL(S)
112
SWITCHABLE
VOLTAGE SUPPLY
CIRCUIT
104
116
VREF1
VREF2
117
118
OUTPUT TO CORE
+
-
VINPUT
102
106
114

FIG. 2

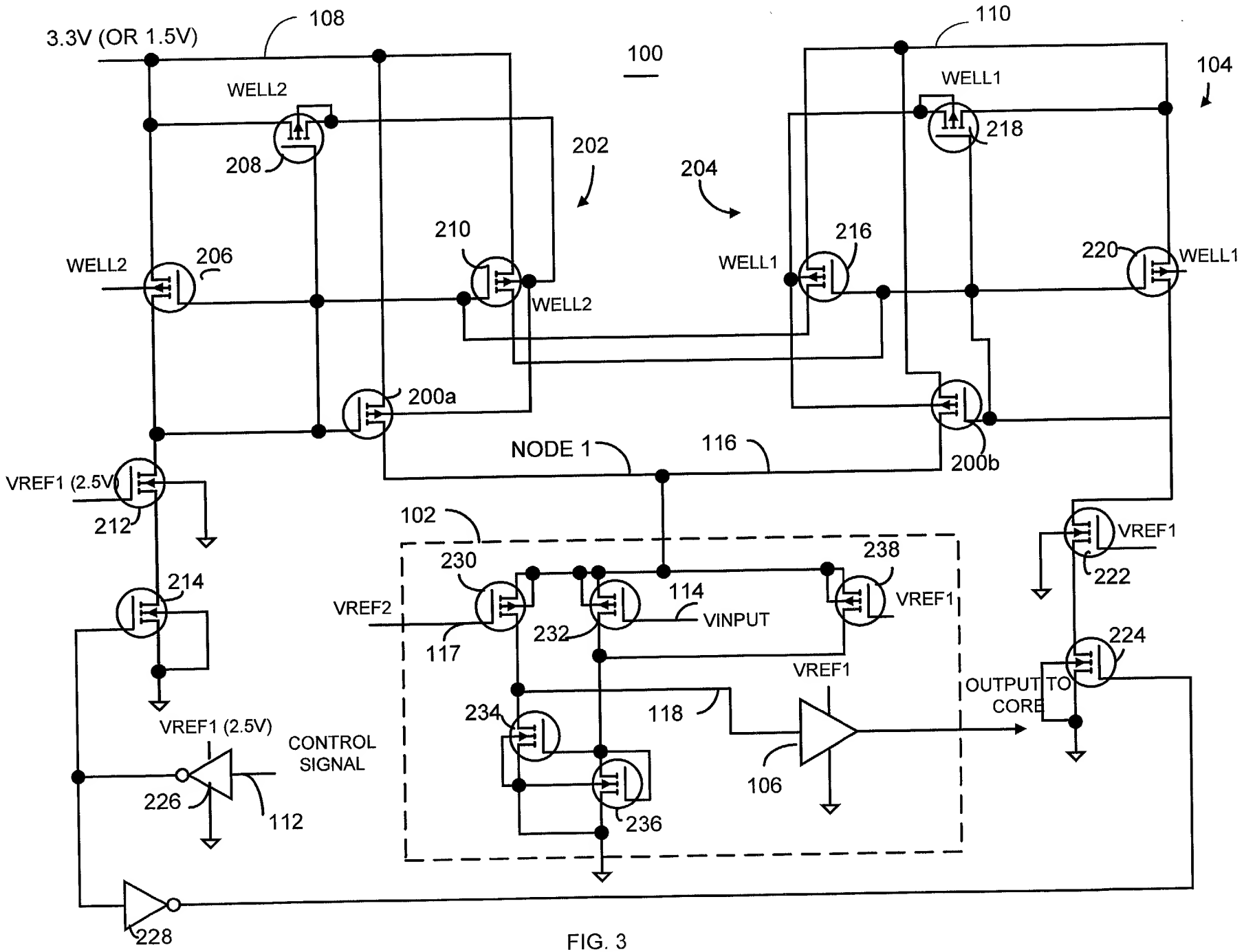
3.3V (OR 1.5V)
108
100
110
104
WELL2
WELL1
208
218
202
204
210
216
220
WELL1
WELL2
206
WELL1
WELL2
200a
200b
NODE 1
116
VREF1 (2.5V)
212
102
VREF1
222
230
238
214
VREF2
114
VINPUT
VREF1
117
232
224
VREF1
OUTPUT TO CORE
234
118
VREF1 (2.5V)
CONTROL SIGNAL
106
226
112
236
228

FIG. 3

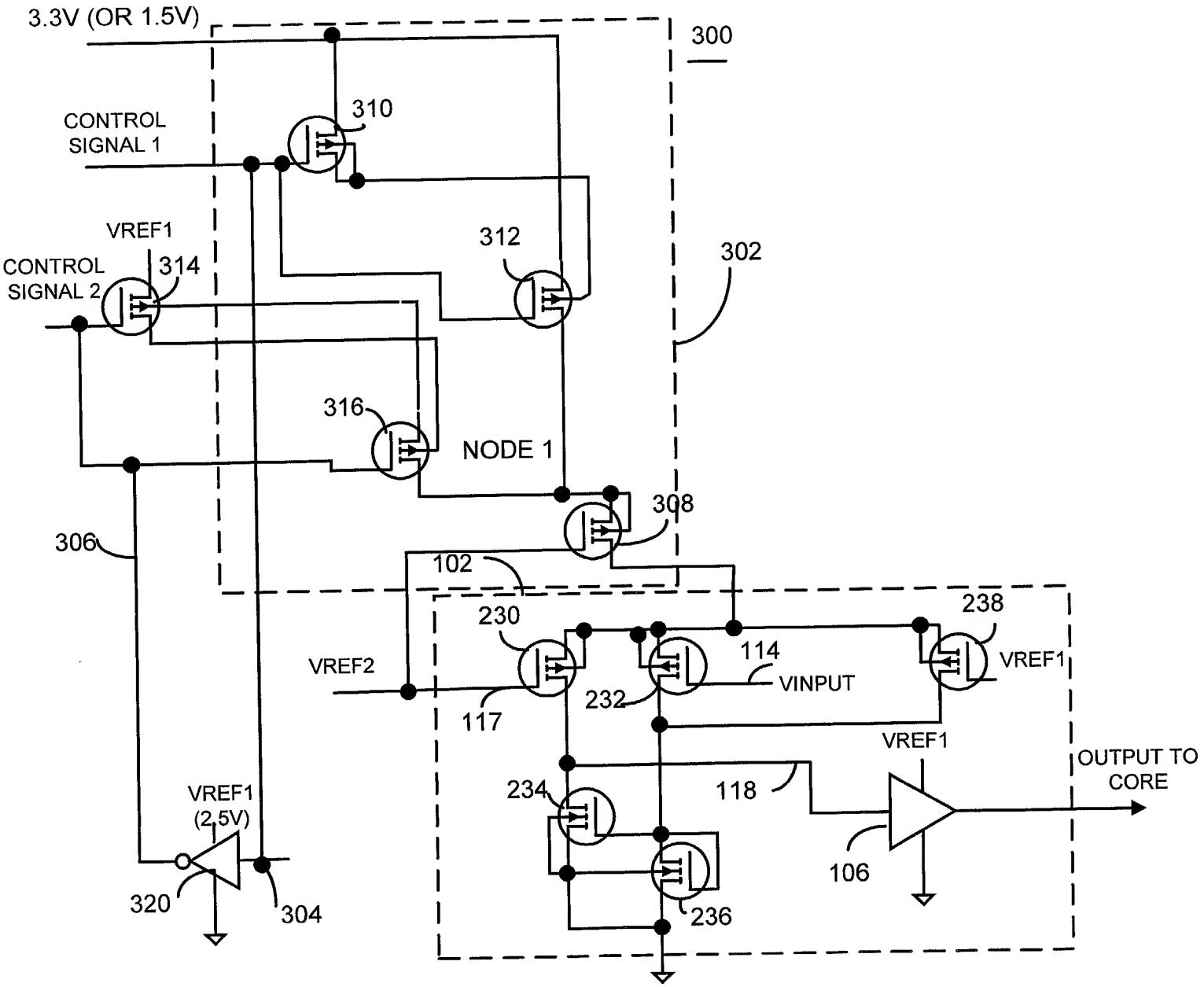
3.3V (OR 1.5V)
300
CONTROL SIGNAL 1
310
VREF1
CONTROL SIGNAL 2
314
312
302
316
NODE 1
308
306
102
230
238
VREF2
114
VINPUT
VREF1
232
117
VREF1
(2.5V)
234
118
OUTPUT TO CORE
320
304
106
236

FIG. 4

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION
(37 CFR 1.63)

☒ Declaration Submitted with Initial Filing, OR
☐ Declaration Submitted after Initial Filing
(surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number 0100.990020
First Named Inventor Oleg Drapkin et al.
COMPLETE IF KNOWN
Application Number
Filing Date
Group Art Unit
Examiner Name

As a below named inventor, I hereby declare that:
My residence, post office address, and citizenship are as stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:
SINGLE GATE OXIDE DIFFERENTIAL RECEIVER AND METHOD
the specification of which:
☒ is attached hereto.
☐ was file on (MM/DD/YYYY) as United States Application Number or PCT International Application Number and was amended on (MM/DD/YYYY) (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Data (MM/DD/YYYY)

☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1 56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Name	Registration Number	Name	Registration Number
Timothy W. Markison	33,534	Christopher J. Reckamp	34,414
Paul M. Anderson	39,896		
Sally Daub	41,478		

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to:

Markison & Reckamp, P.C.
175 West Jackson Boulevard - Suite 1015
Chicago, Illinois 60604
Telephone:312-939-9800
Facsimile: 312-939-9828

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])			Family Name or Surname	
Oleg			**Drapkin**	
Inventor's Signature			**Date**	10.12.98
Residence	**City:North York**	**State: Ontario**	**Country: Canada**	**Citizenship: Israel**
Post Office Address	**6020 Bathhurst Street, No. 905**			
City: North York	**State: Ontario**	**ZIP: M2R 1Z8**	**Country: Canada**	

Name of Additional Joint Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])			Family Name or Surname	
Grigori			**Temkine**	
Inventor's Signature			**Date**	10.12.98
Residence	**City:Toronto**	**State: Ontario**	**Country: Canada**	**Citizenship: Russian**
Post Office Address	**125 Neptune Drive, No. 404**			
City: Toronto	**State: Ontario**	**ZIP: M6A 1X3**	**Country: Canada**	

Name of Additional Joint Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])			Family Name or Surname	
Inventor's Signature			**Date**	
Residence	**City:**	**State:**	**Country:**	**Citizenship:**
Post Office Address				
City:	**State:**	**ZIP:**	**Country:**	

☐ Additional inventors are being named on the _____supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto